

In Re Patent Application of:  
DUBORGEL  
Serial No: 10/035,033  
Filing Date: December 28, 2001

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In the Claims:

This listing of claims replaces all prior versions and listing of claims in the application.

Claims 1-10 (canceled).

11. (Previously presented) A microarchitecture for an arithmetic unit, said arithmetic unit being defined to generate a result of N bits ranked 0 to N-1 of an addition of at least two input operands, and one corresponding output carry bit, said microarchitecture comprising:

an N+1 bit accumulator;

an N+1 bit carry save adder for providing two output vectors from the at least two input operands, one of the operands corresponding to a current contents of the accumulator;

an N+1 bit final adder receiving the output vectors at input and generating a corresponding result at output; and

a determining circuit for receiving a most significant bit of the result generated by said final adder and a most significant bit of the operand corresponding to the current contents of the accumulator and determining the output carry bit.

12. (Previously presented) A microarchitecture of an arithmetic unit according to Claim 11, wherein said carry save adder receives a first operand, a second operand and a third operand as inputs, the third operand corresponding to the current contents of the accumulator; and wherein said

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determining circuit comprises an evaluation circuit for evaluating a most significant bit of a sum of the first and second input operands.

13. (Previously presented) A microarchitecture according to Claim 12, wherein said evaluation circuit comprises an adder for generating the most significant bit of the sum of the first and second input operands.

14. (Previously presented) A microarchitecture according to Claim 12, wherein the determining circuit comprises a logic circuit that outputs the output carry value based upon the most significant bit of the sum of the first and second input operands generated by said evaluation circuit, the N-ranked bit of the current contents of the accumulator and the N-ranked bit of the result generated by the final adder.

15. (Previously presented) A microarchitecture according to Claim 12, further comprising a multiplier for generating partial products of two operands applied as inputs to the arithmetic unit, wherein the partial products are applied as the first and second input operands of the carry save adder.

16. (Previously presented) A microarchitecture according to Claim 12, further comprising a concatenation circuit for the concatenation of two operands input to the arithmetic unit, and generating a concatenated number at

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output, to carry out operations of double precision accumulation with the current contents of the accumulator, the concatenated number being applied as the first input operand of said carry save adder, said second input operand being set at the zero vector.

17. (Previously presented) A microarchitecture according to Claim 15, further comprising:  
a concatenation circuit, connected in parallel with the multiplier, for the concatenation of two operands input to the arithmetic unit, and generating a concatenated number at output, to carry out operations of double precision accumulation with the current contents of the accumulator; and  
a multiplexer connected to the multiplier and the concatenation circuit for selectively applying either the concatenated number and a zero vector or the partial products as the first and second input operands of the carry save adder.

18. (Previously presented) A microarchitecture according to Claim 17, wherein the determining circuit comprises a second multiplexer for selectively providing, as an evaluated bit, either the bit generated by the evaluation circuit or the most significant bit of the concatenated number.

19. (Previously presented) A microarchitecture according to Claim 12, further comprising a format extension circuit for extending the operands applied as first and second

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input operands of the carry save adder to  $N+1$  bits, wherein the evaluation circuit receives the first and second input operands before format extension.

20. (Previously presented) A microprocessor comprising:  
an arithmetic unit for generating a result of  $N$  bits of an addition of at least two input operands, and one corresponding output carry bit, said arithmetic unit comprising

an  $N+1$  bit accumulator;  
an  $N+1$  bit carry save adder for providing two output vectors from the at least two input operands, one of said operands corresponding to a current contents of the accumulator;

an  $N+1$  bit final adder receiving the output vectors at input and generating a corresponding result at output; and

a determining circuit for receiving a most significant bit of the result generated by said final adder and a most significant bit of the operand corresponding to the current contents of the accumulator and determining the output carry bit.

21. (Previously presented) A microprocessor according to Claim 20, wherein said carry save adder receives a first operand, a second operand and a third operand as inputs, the third operand corresponding to the current contents of the accumulator; and wherein said determining

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circuit comprises an evaluation circuit for evaluating a most significant bit of a sum of the first and second input operands.

22. (Previously presented) A microprocessor according to Claim 21, wherein said evaluation circuit comprises an adder for generating the most significant bit of the sum of the first and second input operands.

23. (Previously presented) A microprocessor according to Claim 21, wherein the determining circuit comprises an exclusive-or type logic circuit that outputs the output carry value based upon the most significant bit of the sum of the first and second input operands generated by said evaluation circuit, an N-ranked bit of the current contents of the accumulator and an N-ranked bit of the result generated by the final adder.

24. (Previously presented) A microprocessor according to Claim 21, further comprising a multiplier for generating partial products of two operands applied as inputs to the arithmetic unit, wherein the partial products are applied as the first and second input operands of the carry save adder.

25. (Previously presented) A microprocessor according to Claim 21, further comprising a concatenation circuit for the concatenation of two operands input to the arithmetic unit, and generating a concatenated number at

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output, to carry out operations of double precision accumulation with the current contents of the accumulator, the concatenated number being applied as the first input operand of said carry save adder, said second input operand being set at the zero vector.

26. (Previously presented) A microprocessor according to Claim 24, further comprising:

a concatenation circuit, connected in parallel with the multiplier, for the concatenation of two operands input to the arithmetic unit, and generating a concatenated number at output; and

a multiplexer connected to the multiplier and the concatenation circuit for selectively applying either the concatenated number and a zero vector or the partial products as the first and second input operands of the carry save adder.

27. (Previously presented) A microprocessor according to Claim 26, wherein the determining circuit comprises a second multiplexer for selectively providing, as an evaluated bit, either the bit generated by the evaluation circuit or the most significant bit of the concatenated number.

28. (Previously presented) A microprocessor according to Claim 21, further comprising a format extension circuit for extending the operands applied as first and second input operands of the carry save adder to  $N+1$  bits, wherein the

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evaluation circuit receives the first and second input operands before format extension.

29. (Previously presented) A method of generating a result of N bits of an addition of at least two input operands, and one corresponding output carry bit with an arithmetic unit, the method comprising:

providing an N+1 bit accumulator;

providing two output vectors from the at least two input operands with an N+1 bit carry save adder, one of the operands corresponding to a current contents of the accumulator;

generating the result at an output of an N+1 bit final adder which receives the output vectors at input; and

determining the output carry bit with a determining circuit which receives a most significant bit of the result generated by the final adder and a most significant bit of the operand corresponding to the current contents of the accumulator.

30. (Previously presented) A method according to Claim 29, wherein said carry save adder receives a first operand, a second operand and a third operand as inputs, the third operand corresponding to the current contents of the accumulator; and wherein said determining circuit comprises an evaluation circuit for evaluating a most significant bit of a sum of the first and second input operands.

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31. (Previously presented) A method according to Claim 30, wherein said evaluation circuit comprises an adder for generating the most significant bit of the sum of the first and second input operands.

32. (Previously presented) A method according to Claim 30, wherein the determining circuit comprises an exclusive-or type logic circuit that outputs the output carry value based upon the most significant bit of the sum of the first and second input operands generated by said evaluation circuit, the N-ranked bit of the current contents of the accumulator and the N-ranked bit of the result generated by the final adder.

33. (Previously presented) A method according to Claim 30, further comprising generating partial products of two operands applied as inputs to the arithmetic unit with a multiplier, wherein the partial products are applied as the first and second input operands of the carry save adder.

34. (Previously presented) A method according to Claim 30, further comprising concatenating two operands input to the arithmetic unit with a concatenation circuit to generate a concatenated number which is applied as the first input operand of said carry save adder, said second input operand being set at the zero vector.



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35. (Previously presented) A method according to Claim 33, further comprising:  
concatenating two operands input to the arithmetic unit with a concatenation circuit connected in parallel with the multiplier, to generate a concatenated number; and  
selectively applying either the concatenated number and a zero vector or the partial products as the first and second input operands of the carry save adder with a multiplexer connected to the multiplier and the concatenation circuit.

36. (Previously presented) A method according to Claim 35, wherein the determining circuit comprises a second multiplexer for selectively providing, as an evaluated bit, either the bit generated by the evaluation circuit or the most significant bit of the concatenated number.

37. (Previously presented) A method according to Claim 30, further comprising extending the operands applied as first and second input operands of the carry save adder to  $N+1$  bits with a format extension circuit, wherein the evaluation circuit receives the first and second input operands before format extension.